DSP Software IP Processing Flow and Memory Usage

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Rev B2

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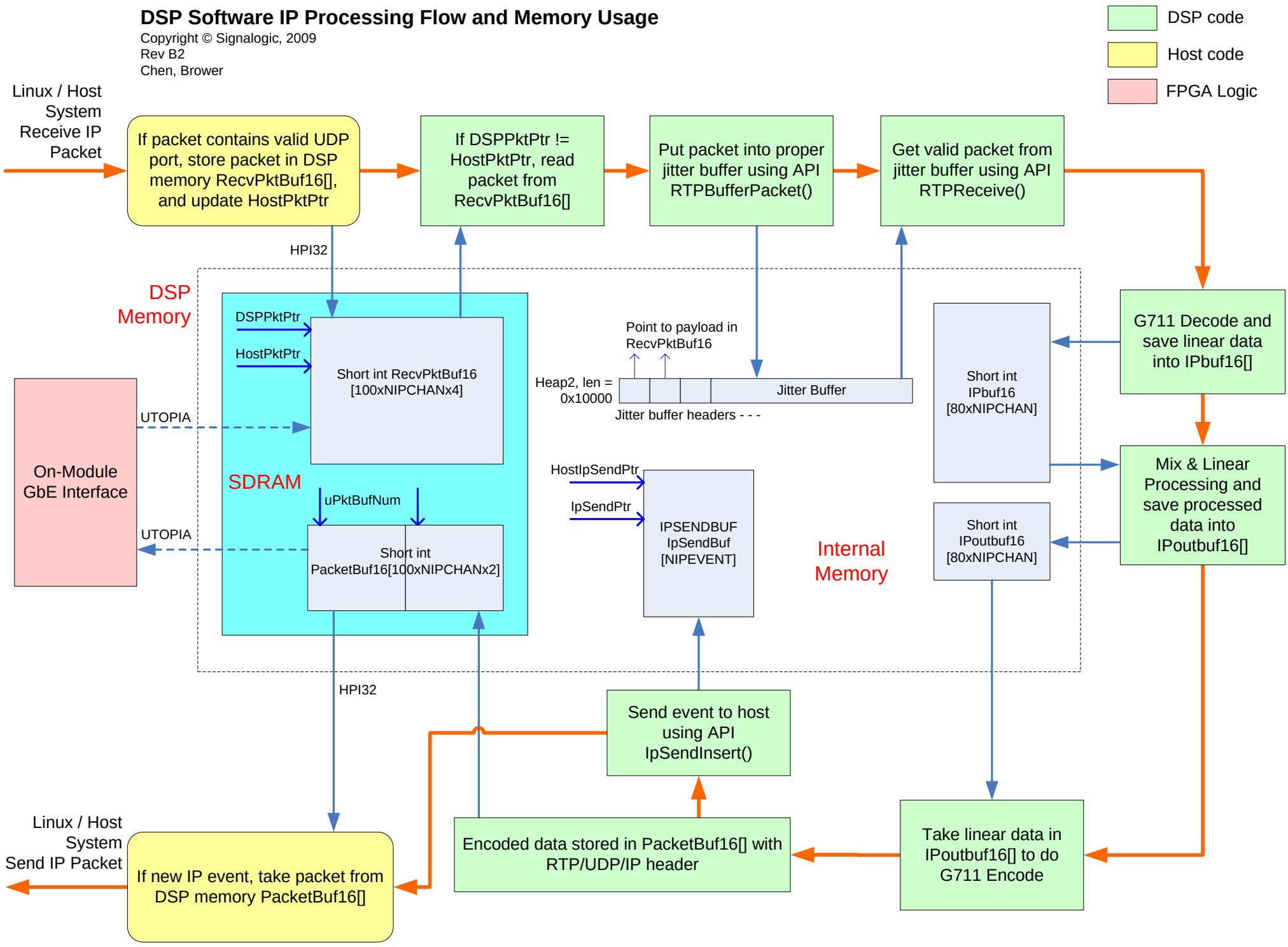
DSP code
Host code
FPGA Logic
Linux / Host System Receive IP Packet
If packet contains valid UDP port, store packet in DSP memory RecvPktBuf16[], and update HostPktPtr
If DSPPktPtr != HostPktPtr, read packet from RecvPktBuf16[]
Put packet into proper jitter buffer using API RTPBufferPacket()
Get valid packet from jitter buffer using API RTPReceive()
HPI32
DSP Memory
DSPPktPtr
HostPktPtr
Short int RecvPktBuf16 [100xNIPCHANx4]
Point to payload in RecvPktBuf16
Heap2, len = 0x10000
Jitter Buffer
Jitter buffer headers - - -
Short int IPbuf16 [80xNIPCHAN]
G711 Decode and save linear data into IPbuf16[]
UTOPIA
On-Module GbE Interface
SDRAM
uPktBufNum
Short int PacketBuf16[100xNIPCHANx2]
HostIpSendPtr
IpSendPtr
IPSENDBUF IpSendBuf [NIPEVENT]
Internal Memory
Short int IPoutbuf16 [80xNIPCHAN]
Mix & Linear Processing and save processed data into IPoutbuf16[]
UTOPIA
HPI32
Send event to host using API IpSendInsert()
Linux / Host System Send IP Packet
If new IP event, take packet from DSP memory PacketBuf16[]
Encoded data stored in PacketBuf16[] with RTP/UDP/IP header
Take linear data in IPoutbuf16[] to do G711 Encode